Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (original): An interconnection system for a plurality of processing elements (PEs), each PE having a communications port for transmitting and receiving data and commands, the interconnection system comprising:

inter-PE connection paths; and

a cluster switch connected to said PEs so as to combine mutually exclusive inter-PE connection paths and to thereby substantially reduce the number of communications paths required to provide inter-PE connectivity equivalent to that of conventional torus-connected PE arrays.

44. (previously presented): An array processor comprising:

a plurality of processing elements arranged in clusters, each cluster including processing elements which communicate in mutually exclusive torus directions with the processing elements of at least one other cluster; and

cluster switches connected to the clusters to provide said mutually exclusive torus direction communication.

45. (previously presented): The array processor of claim 44 wherein each cluster includes an equal number of processing elements.

46. (previously presented): The array processor of claim 44 wherein at least one cluster includes a torus transpose pair of processing elements.

47. (previously presented): The array processor of claim 44 wherein the cluster switches provide inter-PE connectivity equivalent to a torus connected array.

48. (previously presented): The array processor of claim 44 wherein the cluster switches provide direct communication between processing elements in a transpose processing element pair within a cluster.

49. (previously presented): The array processor of claim 44 wherein the clusters of processing elements are scaleable.

50. (previously presented): The array processor of claim 44 wherein the processing elements of each cluster are located in close physical proximity to each other.

51. (previously presented): The array processor of claim 44 further comprising a single instruction multiple data (SIMD) controller which broadcasts data to said plurality of processing elements.

52. (previously presented): The array processor of claim 51 wherein each processing element performs a calculation and transmits the results of the calculation to a nearest neighbor processing element.

53-56. (previously cancelled)

57. (previously presented): The array processor of claim 44 wherein the clusters of processing elements correspond to slices of a torus array shifted and wrapped into a cylinder.

58. (previously presented): The array processor of claim 44 wherein each processing element (PE) is defined as $PE_{i,j}$, where i and j refer to the respective row and column PE positions within a conventional torus-connected array, and where i = 0,1,2, ... N-1 and j = 0, 1, 2, . . . N-1, said PEs arranged in clusters $PE_{(i+a)(ModN),(j+N-a)(ModN)}$, for any i,j and for all a $\in$ {0,1,...,N-1}.

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59. (previously presented): The array processor of claim 44 wherein each cluster switch multiplexes communications from processing elements within a cluster for transmission to another cluster.